Amdt PATENT APPLICATION 2818

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Koichi MIZUGAKI et al.

Application No.: 09/976,021

Filed: October 15, 2001 Docket No.: 110827

For: ACTIVATION OF WORD LINES IN SEMICONDUCTOR MEMORY DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. The references were cited in a counterpart foreign office action. An English language version of the foreign office action is attached for the Examiner's information. (Refs. 1-5)

☒ 3. English-language Abstracts of the non-English language references are attached hereto. (Refs. 1-5)

☒ 4. A computer-generated English translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See References 1-5.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Thomas J. Pardini
Registration No. 30,411

JAO:TJP/amo

Date: April 21, 2004

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 110827	APPLICATION NO. 09/976,021
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANTS Koichi MIZUGAKI et al.	
		FILING DATE October 15, 2001	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1	JP A 5-250867 w/ abst & trans	09/28/1993	Japan		
	2	JP A 8-129882 w/ abst & trans	05/21/1996	Japan		
	3	JP A 11-306753 w/ abst & trans	11/05/1999	Japan		
	4	JP A 2003-074944 w/ abst & trans	03/12/2003	Japan		
	5	JP A 2003-085970 w/ abst & trans	03/20/2003	Japan		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: April 21, 2004

Dispatch Date: February 10, 2004

NOTIFICATION OF REASON FOR REJECTION

Patent Application No. 2000-328110

Drafting Date	February 2, 2004
Examiner of JPO	Kazuyoshi Hotta 8840 5N00
Representative/Applicant	Takao Igarashi (and three others)
Applied Provision	Patent Law Section 29(2)

The application should be refused for the reason mentioned below. If the applicant has any argument against the reason, such argument should be submitted within 60 days from the date on which this notification was dispatched.

Reason

The inventions in claims 1-5 of the subject application should not be granted a patent under the provision of Patent Law Section 29(2) since they could have easily been made by persons who have common knowledge in the technical field to which the inventions pertain, on the basis of the inventions described in the publications listed below which were distributed in Japan or foreign countries or the inventions were made available to the public through electric communication lines prior to the filing of the subject application.

Notes

Cited Publication 1: JP 11-306753A
Cited Publication 2: JP 4-106782A
Cited Publication 3: JP 5-250867A
Cited Publication 4: JP 5-325544A
Cited Publication 5: JP 4-132075A
Cited Publication 6: JP 8-129882A
Cited Publication 7: JP 5-182452A

[With regard to the invention of Claim 1]

1. See the paragraphs [0054] to [0056] and [Fig.6] in Cited Publication 1.

Cited Publication 1 describes that when a refresh request for a first sub-array is made during page mode operation for the first sub-array being

executed, an activated word line WLi is deactivated prior to the refresh being performed.

The invention of claim 1 and the invention of Cited Publication 1 (hereinafter referred to as 'cited invention') are different in that the former includes a row address transition detector, and when the row address transition detector does not detect a change in a row address during consecutive cycles, maintains an activated status of a word line activated during a first cycle of the consecutive cycles without deactivating the word line until a final cycle of the consecutive cycles while the latter does not include a row address transition detector, and resets a word line activated during a first cycle of consecutive cycles after a predetermined period of time.

The above difference is discussed below..

As described in Cited Publication 2 (Fig. 15) and in Cited Publications 3 to 5, it is a well known technique that a semiconductor storage device includes a row address transition detector, and when the row address transition detector does not detect a change in a row address during consecutive cycles, maintains an activated status of a word line activated during a first cycle of the consecutive cycles without deactivating the word line until a final cycle of the consecutive cycles. Therefore, a person skilled in the art could have readily apply the well known technique to the cited invention in order to arrive at the invention of claim 1 that includes a row address transition detector, and when the row address transition detector does not detect a change in a row address during consecutive cycles, maintains an activated status of a word line activated during a first cycle of the consecutive cycles without deactivating the word line until a final cycle of the consecutive cycles.

[With regard to the invention of Claim 2]

2. There is not any noticeable difficulty in assigning a row address to a plurality of uppermost bits of an address.

[With regard to the invention of Claim 3]

3. See the paragraph [0038] and [Fig. 7] in Cited Publication 3. There is not any difficulty in maintaining an activated status of a word line in a first memory block while maintaining an activated status of a word line in a second memory block.

[With regard to the invention of Claim 4]
4. See the description of claim 4 in Cited Publication 1.
See also [Fig. 13] to [Fig. 16] in Cited Publication 6 and [Fig. 4] in Cited Publication 7.

[With regard to the invention of Claim 5]
5. The invention of claim 5 is only a variation obtained by changing the category of the invention of claim 1 from device to method.

Record of the result of prior art search

Searched field	IPC Version 7	G11C11/403
	DB Name	
Prior art document	JP 2003-85970A	
	JP 2003-74944A	

This record of the result of prior art search does not constitute the Reason for Rejection.